

## FAST SYMBOL TIMING RECOVERY FOR TRANSMITTED DIGITAL DATA

### CROSS-REFERENCE TO RELATED APPLICATIONS

5           This application claims priority of Provisional Application serial no. 60/425,781 of the same title filed on November 12, 2002.

### FIELD OF THE INVENTION

10           This invention relates generally to receiver synchronization upon receipt of a broadband transmission, and more particularly, to symbol synchronization at the receiver upon receipt of a broadband transmission having a high bit rate.

### DESCRIPTION OF THE RELATED ART

15           A Time-Division Duplex (TDD) or Time Division Multiple Access (TDMA) transmission system is one which sends and receives information, for example in the form of packets, at different times. Such a TDD or TDMA system requires that symbol timing be accurately recovered for each packet, especially at the beginning of the packet where typically a sync-word and header are stored. Such a circumstance is encountered in a twisted-pair broadband connection, such as digital subscriber loop, between customer premises equipment (CPE) and a  
20           central office (CO). If the CPE and CO modems have a different digital oscillators for their clock signals and no constant and reliable clock signals are interchanged, a difference in their digital oscillators of 50 PPM (0.005%) over a transmission receiving period of 2000 us, causes a maximum timing difference of 0.1 us. If the symbol rate in the transmission system is 7 million baud, the symbol period is 0.143 us. Therefore, such a timing difference (about 70%) would  
25           create a huge error in the first part of a received packet. At the very least the sync word of the packet would be lost.

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In TDD or TDMA systems, there are several ways to achieve symbol timing recovery. One is a line-locked clock found in the signals. This requires a pre-equalization signal which can be greatly distorted due to line conditions such as a tap-bridge or cross-talk. The pilot signal in a packet would be vulnerable to loss. Normally, a phase lock loop (PLL) must be implemented in such systems.

Alternatively, the symbol's timing can be recovered by re-training a receiver equalizer each time a packet is received and the symbol timing can be derived from the signals after equalization because the post-equalization signals would have very little distortion. This scheme only applies to low bit rate situations where the DSP and equalization functions can be implemented by using software/firmware means and data can be re-processed.

Yet other alternatives are that a very long pilot can be used, resulting in very high overhead or a receiver equalizer with relatively few taps can be used making it faster to retrain while sacrificing the quality of the equalizer function.

However, the above solutions are unacceptable for a digital subscriber loop (DSL) which has a high symbol rate and a high bit rate. The solutions based on software/firmware only are simply not viable.

Therefore, there is a need, in a high symbol rate time domain (TD) system, for the fast recovery of symbol timing at the receiver.

## BRIEF SUMMARY OF THE INVENTION

The present invention provides for fast recovery of symbol timing at the receiver without excessive pilot length or equalizer retraining. A method, in accordance with the present invention, allows for rapidly recovering symbol synchronization for a serial transmission. The method includes the steps of (i) obtaining in-phase and quadrature components of a received digital bitstream, where the components include a pilot bitstream that is embedded in the received components; (ii) storing a copy of the obtained in-phase and quadrature components; (iii) recovering a version of the pilot bitstream from the obtained components; (iv) computing a timing correction factor based on the recovered pilot bitstream; (v) if the timing correction factor is non-zero, applying the timing correction factor to the stored copy of the received components to adjust the symbol timing of the received bitstream; and (vi) recovering another version of the pilot bitstream from the copy of the received bitstreams based on the adjusted symbol timing.

The present invention quickly accomplishes symbol timing recovery because the timing correction factor becomes a small number with only a few iterations of the above method.

A high speed TD system becomes feasible when the present invention is employed because symbol timing recovery, which is required on each new reception, is fast.

5 Further, implementation of the present invention can be carried out using existing digital signal processing techniques such as filters, equalizers, and memory.

## BRIEF DESCRIPTION OF THE DRAWINGS

10 These and other features, aspects and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where:

FIG. 1 shows the transmissions in a TD system;

FIG. 2 shows a block diagram of the fast recovery system;

15 FIG. 3 shows a more detailed diagram of the Fast Timing Equalizer, the Synchronization Block and the 8 to 3 interpolation blocks;

FIG. 4 shows a flow chart of the symbol timing recovery procedure;

FIG. 5 shows a diagram of the conceptual operation of the reflection buffer;

FIG. 6a shows the waveshape of the signal bits for the pilot, P;

FIG. 6b is a table of the modified BARC code which comprises the pilot waveform;

20 FIG. 6c is the plotted pilot waveform resulting from programming the code into the registers;

FIG. 6d shows the spectrum of the waveshape of the pilot signal bits;

FIG. 6e shows the waveshape of the signal bits for the mirrored pilot, P';

FIG. 6f is a table of the modified BARC code which comprises the P' waveform;

25 FIG. 6g is the plotted pilot waveform resulting from programming the code into the registers for the P' waveform; and

FIG. 7 shows the resulting structure of a frame in accordance with the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

30 FIG. 1 shows exemplary transmissions in a TD system for the CO and CPE elements. As shown, each element times transmission and reception periods substantially opposite to the

corresponding element. During the transmission period for a first element in block 10, the other element is in a receive period in block 12. The first element then has a receive period, block 14 corresponding to the other element's transmit period in block 16. Exemplary division of the periods for multiplexing is shown with the RX1, RX2, etc. division of the receive period in block 18. The difference in timing which may be present between the two elements is demonstrated by offset 20

FIG. 2 shows a block diagram of the fast recovery system. Included are an Analog Front End (AFE) 22, a Demodulator with automatic gain control (AGC) 24 and the timing recovery element 26 which includes the functions of a Fast Timing Equalizer 28, an M-to-N Interpolation and Timing Adjustment Block 30, and a pilot detection block 32. The Demodulator operates on the modulated QAM broadband signal to produce the in-phase and quadrature components of the QAM signal. The fast timing equalizer is designed, in conjunction with the Final Equalizer, to minimize intersymbol interference (ISI) introduced by the transmitter and channel frequency characteristics. The 8 to 3 Interpolator down converts the timing from  $T_s/8$  to  $T_s/3$ , where  $T_s$  is the symbol rate. The pilot signal and detection block are designed to accurately and quickly recover symbol timing for the received data, and is more fully described below.

FIG. 3 shows a more detailed diagram of the timing recovery element demonstrating the interrelationship of the Fast Timing Equalizer, Pilot Signal Correlator which acts as the pilot detector and the 8 to 3 Interpolation blocks which adjusts the timing. Also included is a reflection buffer 34 which stores incoming data to provide to the interpolator, fast equalizer, and pilot correlator. Data is received by the reflection buffer at  $T_s/8$  ( $8 \times F_s$ ) and then fed to the interpolator/phase adjuster acting as a down sampler which changes the rate to  $T_s/3$  ( $3 \times F_s$ ). The data is then fed to the fast equalizer and then to a pilot correlator. The interpolator, the equalizer and the reflection buffer each received feedback from the pilot correlator.

The interpolator is used to perform phase adjustment. The fast equalizer after the interpolator reduces the channel distortion to improve the pilot correlation and detection function and to help the final data detection in the final equalizer. The total equalization in the system is the concatenation of the fast equalizer and the final equalizer. The fast equalizer has 24 (or less) taps and is controlled and trained by the pilot correlator.

The pilot correlator is designed to find the pilot with great precision such that the incoming pilot can be better-received by the main equalizer and subsequent modules, as will be described in greater detail subsequently.

Referring to FIG. 4, in step 40,  $I\_data(n)$ ,  $Q\_data(n)$ , are received from the I and Q demodulators, respectively, in the demodulation block of FIG. 1. The demodulation block receives the broadband DSL Differential Phase-Shift Keying (DPSK) pilot signal and Quadrature Amplitude Modulated (QAM) signal containing the symbol stream to be recovered. Next, in step 42, the sampled  $p(n)$  data for the pilot signal is retrieved from storage. The  $p(n)$  data has a baseband spectrum that matches the expected spectrum of the pilot input signal. The  $I\_data(n)$ ,  $Q\_data(n)$  and  $p(n)$  data are then sent to the pilot correlator, which is a match filter designed to maximize the output signal over the rms noise level. If the noise is white noise, then convolving the input with the spectrum of the expected input, e.g.,  $p(n)$ , generates this result. In steps 44 and 46, the  $I\_data(n)$  and  $Q\_data(n)$  are convolved (Eq. 1 and 2) with the sampled version of the predefined pilot signal  $p(n)$ , whose characteristics are described in detail below.

$$Ip(n) = \sum p(i) * I\_data(n-i) \quad (1)$$

$$Qp(n) = \sum p(i) * Q\_data(n-i) \quad (2)$$

$$I'p(n) = \sum p'(i) * I\_data(n-i) \quad (3)$$

$$Q'p(n) = \sum p'(i) * Q\_data(n-i) \quad (4)$$

The outputs of pilot correlator,  $Ip(n)$ ,  $Qp(n)$ ,  $I'p(n)$ ,  $Q'p(n)$  are combined according to equations 5 and 6, in step 48, after taking the absolute value of each output,

$$C(n) = abs(Ip(n)) + abs(Qp(n)) \quad (5)$$

$$C'(n) = abs(I'p(n)) + abs(Q'p(n)) \quad (6)$$

and each sum  $C(n)$ ,  $C'(n)$  is compared, in step 50, to a predefined threshold T. If the output  $C(n)$  is greater than the threshold T and is the largest of the last 48 outputs, as defined in step 52, then the pilot signal P is considered detected. Alternatively, if there is more than one pilot signal P in the input bit stream, then if the last event detected is greater than the predefined threshold and the largest of the last 48 outputs, P is considered detected.

Detection of P' is slightly different from detection of P. Equations 3 and 4 must be met, but the sign of  $I_{p'}(n)$  and  $Q_{p'}(n)$  for P' must be opposite to the sign of  $I_p(n)$  and  $Q_p(n)$  for P. Alternatively, if  $\{I_p(n), Q_p(n)\}$  is orthogonal to  $\{I_{p'}(n), Q_{p'}(n)\}$ , then P' is considered detected.

Once P and P' are detected, a timing correction is calculated, in step 54,

$$\Delta = \frac{C(i-1) - C(i+1)}{(C(i)/8)} \quad (7),$$

where  $C(n)$  is the output of the pilot correlator and  $n$  is the index for maximal output. If the symbol timing is correct,  $C(i)$  is a maximum and  $C(i-1)$  and  $C(i+1)$  are equal because they are symmetric about the maximum. Otherwise, equation 7 computes a correction to the symbol timing, either positive or negative, which is used in a loop to reduce the symbol timing error. In this loop, a first set of P and P' inputs and two sets of saved P and P' inputs from the reflection buffer are sent to the pilot correlator in step 56 and a timing correction is calculated. If the symbol period is 143 nanoseconds (ns), the timing error has been reduced to approximately  $T_s/16$  (about 9 ns or 6 %) after the second iteration of the loop, and to approximately  $T_s/32$  (about 4.4 ns or 3 %) after the third iteration of the group. In each iteration of the loop the timing adjustment is used to offset the pointer in the reflection buffer by an amount equal to  $\Delta$ .

FIG. 5 shows a diagram of the conceptual operation of the reflection buffer. In the first pilot detection position 58, the input to the correlator is derived from the demodulated data stream. In the second detection position 60, the pointer is reset and the pilot is again input to the correlator from the reflection buffer. In the third detection position 62, the pointer is again reset and the pilot and data input to the correlator is derived from the reflection buffer. The pointer to the data in the reflection buffer is altered based on the timing error computed above.

FIG. 6a is an example of the pilot waveform. The pilot shown has all the frequency components and cannot be corrupted totally by the channel. For the embodiment shown, the pilot is 16 symbols in length having broad spectrum coverage and high AC energy. The pilot is implemented using the QAM cosine filter. The generated I and Q signals have opposite polarity which enhances the detection operation. The pilot is a Modified BARC code with the patterns shown in FIG. 6b. The pilot code can be programmable by writing to the registers of the system. FIG. 6c is a plot of the resulting pilot waveform. FIG. 6d shows a spectrum of the pilot signal. A discrete version of this spectrum is used by the pilot correlator to help recover the correct symbol timing.

For the embodiments shown, P' is a mirror image of P as shown in FIG. 6e. Again a modified BARC code with the patterns shown in FIG. 6f is employed to create the code for P' while FIG. 6g shows the resulting waveform.

5 After the pilot signal has been reliably detected, the pilot correlator becomes a phase adjuster, i.e., an all pass filter with pre-calculated coefficients, and the fast (24 tap) equalizer is adjusted by updating its coefficients.

FIG. 7 shows the structure of a resulting frame using the reflection buffer in accordance with the present invention. The pilot is detected a first time in blocks 64 after which the timing correction  $\Delta$  is inserted, a second time after timing adjustment in blocks 66 after which the  
10 timing correction has been reduced to  $\delta$  and a third time in blocks 68 preceding the sync word 70 and data stream 72 being received. The timing error has been reduced in the data stream to  $\epsilon$  which is nominally smaller than  $T_s/32$ . The pilot signal portion is transmitted according to Differential Phase Shift Keying (DPSK) and the sync and data fields are transmitted using Quadrature Amplitude Modulation (QAM).

15 Although the present invention has been described in considerable detail with reference to certain preferred versions thereof, other versions are possible. Therefore, the spirit and scope of the invention should not be limited to the description of the preferred versions contained herein. Having now described the invention in detail as required by the patent statutes, those skilled in the art will recognize modifications and substitutions to the specific embodiments  
20 disclosed herein. Such modifications are within the scope and intent of the present invention as defined in the following claims.